MIC28514

75V/5A Hyper Speed Control®
Synchronous DC/DC Buck Regulator with External Soft Start

Features

- Hyper Speed Control® Architecture Enables:
  - High Input to Output Voltage Conversion Ratio Capability (V_{IN} = 75V and V_{OUT} = 0.6V)
  - Small Output Capacitance
- 4.5V to 75V Input Voltage
- 5A Output Current Capability with up to 95% Efficiency
- Adjustable Output Voltage from 0.6V to 32V
- ±1% FB Accuracy
- Any Capacitor™ Stable:
  - Zero-ESR to High-ESR Output Capacitors
- 270 kHz to 800 kHz Adjustable Switching Frequency
- Internal Compensation
- Built-in 5V Regulator for Single-Supply Operation
- Auxiliary Bootstrap LDO for Improving System Efficiency
- Internal Bootstrap Diode
- Adjustable Soft Start Time
- Programmable Current Limit
- “Hiccup” Mode Short-Circuit Protection
- Thermal Shutdown
- Supports Safe Start-up into a Prebiased Output
- -40°C to +125°C Junction Temperature Range
- Available in 32-Pin, 6 mm x 6 mm VQFN Package

Applications

- Distributed Power Systems
- Communications/Networking Infrastructure
- Industrial Power Supplies
- Solar Energy

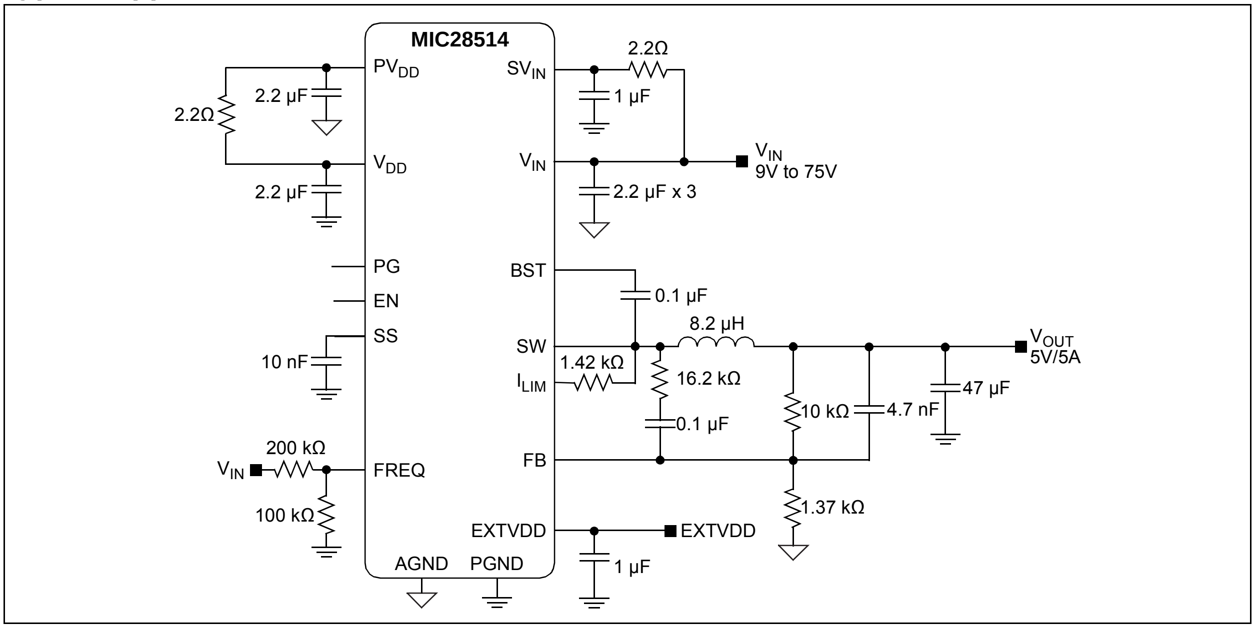
General Description

The MIC28514 is an adjustable frequency, synchronous buck regulator that features a unique adaptive on-time control architecture. The MIC28514 operates over an input supply range of 4.5V to 75V, and provides a regulated output of up to 5A of output current. The output voltage is adjustable down to 0.6V with an accuracy of ±1%.

Hyper Speed Control architecture allows for an ultra-fast transient response, while reducing the output capacitance, and also makes high-V_{IN}/low-V_{OUT} operation possible. This adaptive on-time control architecture combines the advantages of fixed frequency operation and fast transient response in a single device.

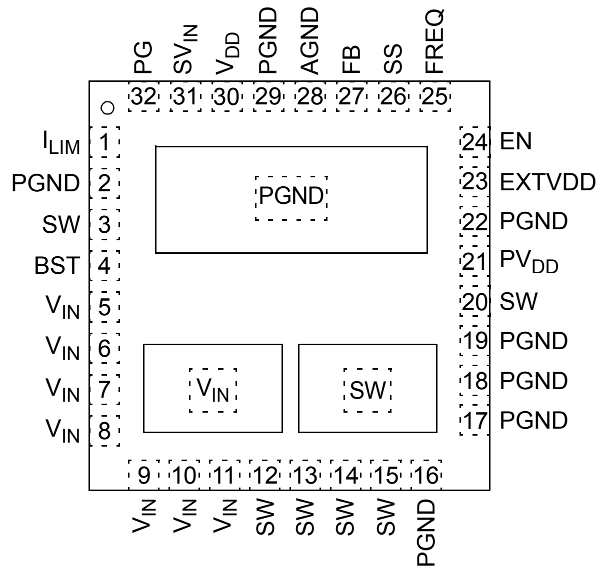
The MIC28514 offers a full suite of features that ensure the protection of the Integrated Circuit (IC) during Fault conditions. These features include Undervoltage Lockout (UVLO) to ensure proper operation under power sag conditions, soft start to reduce inrush current, “Hiccup” mode short-circuit protection and thermal shutdown.

Typical Application Circuit

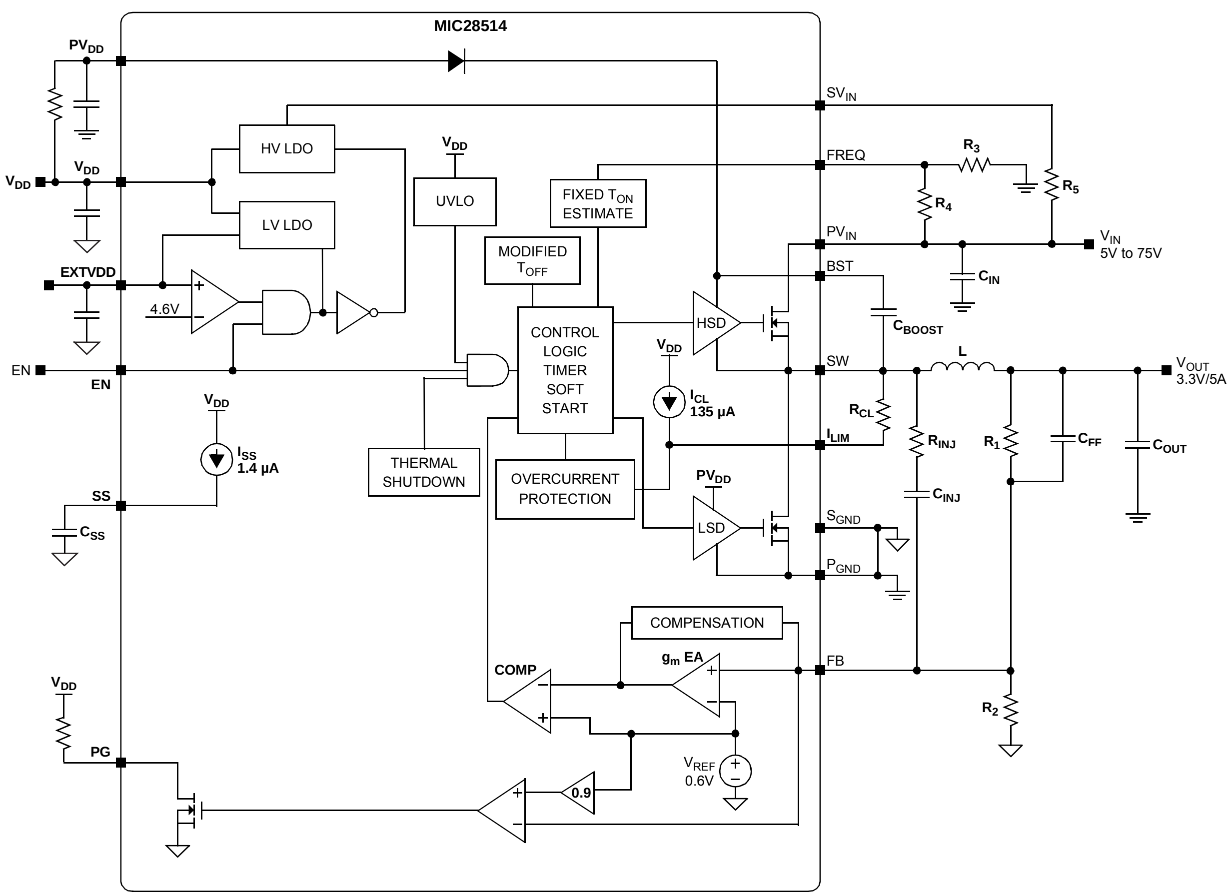


Package Type

MIC28514
6 mm x 6 mm 32-Lead VQFN



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

PV_{IN}, SV_{IN}, FREQ to PGND .... -0.3V to +76V
PV_{DD}, V_{DD} to PGND .... -0.3V to +6V
SW, I_{LIM} to PGND .... -0.3V to (PV_{IN} + 0.3V)
V_{BST} to V_{SW} .... -0.3V to +6V
V_{BST} to PGND .... -0.3V to +82V
EN to AGND .... -0.3V to (SV_{IN} + 0.3V)
FB, PG to AGND .... -0.3V to (V_{DD} + 0.3V)
EXTVDD to AGND .... -0.3V to +12V
PGND to SGND .... -0.3V to +0.3V
Junction Temperature .... +150°C
Storage Temperature .... -65°C to +150°C
ESD Rating(1) .... 1 kV

Operating Ratings‡

Supply Voltage (SV_{IN}, PV_{IN}) .... 4.5V to 75V
Bias Voltage (PV_{DD}, V_{DD}) .... 4.5V to 5.5V
EN, FB, PG .... 0V to V_{DD}
EXTVDD 0V to12V
Junction Temperature .... -40°C to +125°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not ensured to function outside its operating ratings.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS(1)

Electrical Characteristics: PV_{IN} = 12V, V_{OUT} = 5V, V_{DD} = 5V, $V_{BST} – V_{SW}$ = 5V; f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH; T_A = +25°C, unless noted. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	PV_{IN}, SV_{IN}	**4.5**	—	**75**	V	
V_{DD} Bias Voltage						
Operating Bias Voltage	V_{DD}	**4.8**	5.1	**5.4**	V	
Undervoltage Lockout Trip Level	UVLO	**3.7**	4.2	**4.6**	V	V_{DD} rising
UVLO Hysteresis	UVLO_HYS	—	600	—	mV	
V_{DD} Dropout Voltage		700	—	1250	mV	V_{IN} = 5.5V, I_{PVDD} = 25 mA
EXTVDD Switchover Voltage		**4.4**	4.6	**4.8**	V	
EXTVDD Switchover Hysteresis		—	0.2	—	V	
Quiescent Supply Current	I_Q	—	1.25	—	mA	V_{FB} = 1.5V
Shutdown Supply Current	I_{QSHDN}	—	0.15	**2**	µA	Power from V_{IN}, V_{EN} = 0V
		—	35	**60**	µA	V_{IN} = V_{DD} = 5.5V, V_{EN} = 0V

Note 1: Specification for packaged product only.
2: The I_{CL} is trimmed to get the current in the limits at room temperature.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[(1)] (CONTINUED)

Electrical Characteristics: PV_{IN} = 12V, V_{OUT} = 5V, V_{DD} = 5V, $V_{BST} – V_{SW}$ = 5V; f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH; T_A = +25°C, unless noted. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Reference						
Feedback Reference Voltage	V_{FB}	**0.597**	0.6	**0.603**	V	T_J = +25°C
		0.594	0.6	**0.606**		-40°C ≤ T_J ≤ +125°C
Load Regulation	—	—	0.04	—	%	I_{OUT} = 0A to 5A
Line Regulation	—	—	0.1	—	%	PV_{IN} = 7V to 75V
FB Bias Current	I_{FB_BIAS}	**—**	0.05	**0.5**	µA	V_{FB} = 0.6V
Enable Control						
EN Logic Level High	EN_{HIGH}	**1.6**	—	—	V	
EN Logic Level Low	EN_{LOW}	—	—	**0.6**	V	
EN Bias Current	I_{ENBIAS}	—	6	**30**	µA	V_{EN} = 0V
On Timer						
Maximum Switching Frequency	FREQ	720	800	880	kHz	FREQ = PV_{IN}, I_{OUT} = 5A
Minimum Switching Frequency	FREQ	**230**	270	**300**	kHz	FREQ = 33% PV_{IN}
Maximum Duty Cycle	D_{MAX}	—	85	—	%	V_{FB} = 0V, FREQ = PV_{IN} (**Note 1**)
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{FB} > 0.6V
Minimum Off-Time	$t_{OFF(MIN)}$	100	200	**300**	ns	
Minimum On-Time	$t_{ON(MIN)}$		60	—	ns	
Soft Start						
Soft Start Current Source	I_{SS}	**0.8**	1.4	**3**	µA	
Soft Start Period Range	—	**2.5**		**40**	ms	
Current Limit						
Current Limit	I_{CLIM}	5.75	6.25	6.75	A	R_{CL} = 1.42 kΩ (**Note 2**)
I_{LIM} Source Current	I_{CL}	—	135	—	µA	
I_{LIM} Source Current Tempco	—	—	0.3	—	µA/°C	
Internal FETs						
Top MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$	—	25	—	mΩ	
Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$	—	25	—	mΩ	
SW Leakage Current	I_{SWLEAK}	—	—	**5**	µA	PV_{IN} = 48V, V_{EN} = 0V
PV_{IN} Leakage Current	$I_{VINLEAK}$	—	—	**10**	µA	PV_{IN} = 48V, V_{EN} = 0V
BST Leakage Current	$I_{BSTLEAK}$	—	—	**10**	µA	PV_{IN} = 48V, V_{EN} = 0V
Power Good (PG)						
PG Threshold	V_{PG_TH}	**85**	90	**95**	%	V_{FB} rising
PG Threshold Hysteresis	V_{PG_HYS}	—	6	—	%	V_{FB} falling
PG Delay Time	t_{PG_DLY}	—	100	—	µs	V_{FB} rising
PG Low Voltage	V_{PG_LOW}	—	70	**200**	mV	V_{FB} < 90% × V_{NOM}, I_{PG} = 1 mA
Thermal Protection						
Overtemperature Shutdown	T_{SHD}	—	150	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	T_{SHD_HYS}	—	15	—	°C	

Note 1: Specification for packaged product only.

2: The I_{CL} is trimmed to get the current in the limits at room temperature.

TABLE 1-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	-40	—	+125	°C	(**Note 1**)
Storage Temperature Range	T_S	-65	—	+150	°C	
Junction Temperature	T_J	—	—	+150	°C	
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistance						
Thermal Resistance, 6 mm x 6 mm, QFN-32LD	θ_{JA}	—	33.3	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL CHARACTERISTIC CURVES

> **Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

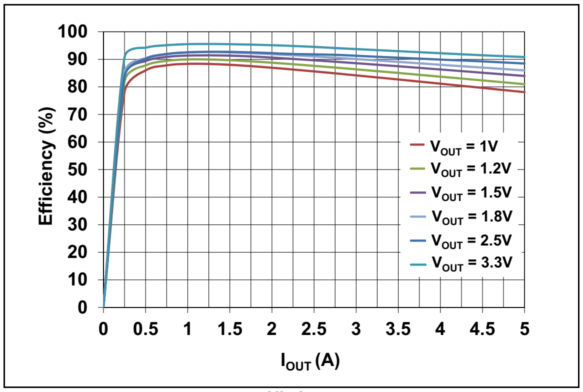


FIGURE 2-1: *Efficiency vs. Output Current (V_{IN} = 5V).*

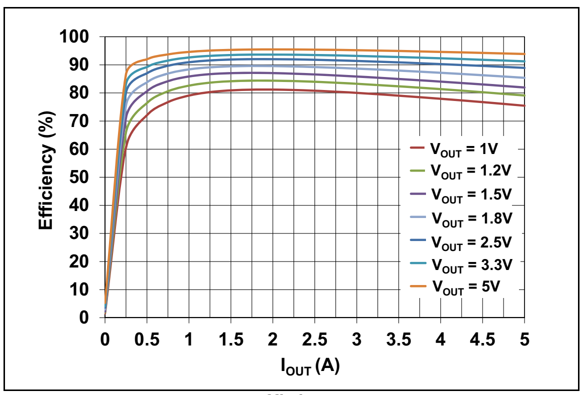


FIGURE 2-2: *Efficiency vs. Output Current (V_{IN} = 12V).*

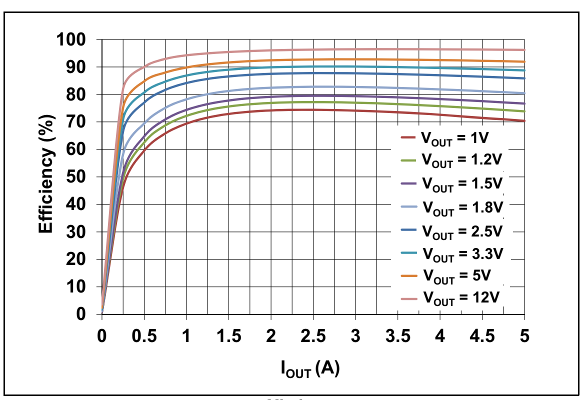


FIGURE 2-3: *Efficiency vs. Output Current (V_{IN} = 24V).*

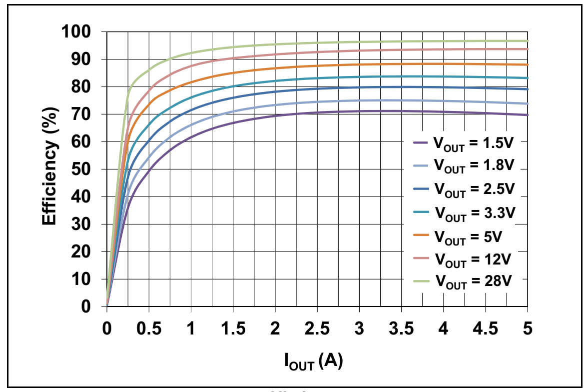


FIGURE 2-4: *Efficiency vs. Output Current (V_{IN} = 48V).*

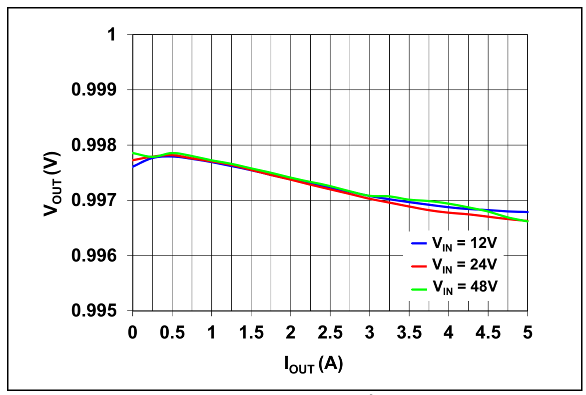


FIGURE 2-5: *Output Voltage vs. Output Current (V_{OUT} = 1V).*

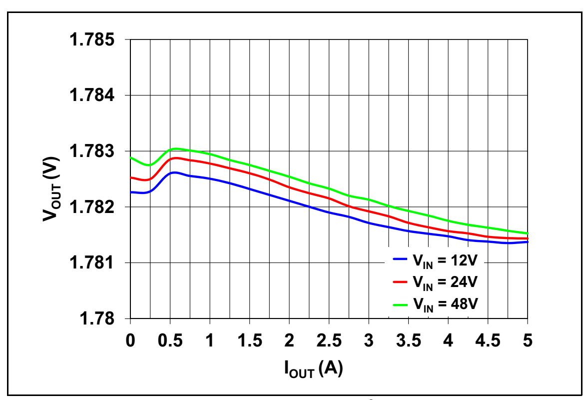


FIGURE 2-6: *Output Voltage vs. Output Current (V_{OUT} = 1.8V).*

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

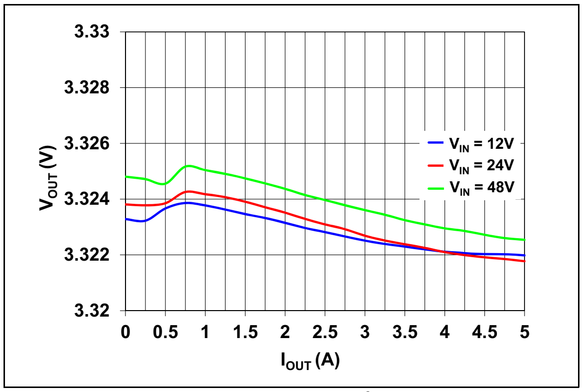


FIGURE 2-7: *Output Voltage vs. Output Current (V_{OUT} = 3.3V).*

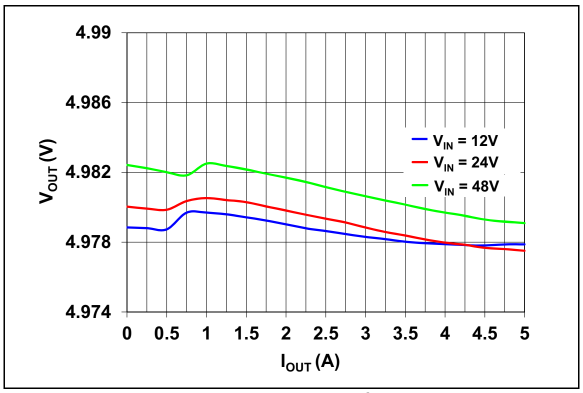


FIGURE 2-8: *Output Voltage vs. Output Current (V_{OUT} = 5V).*

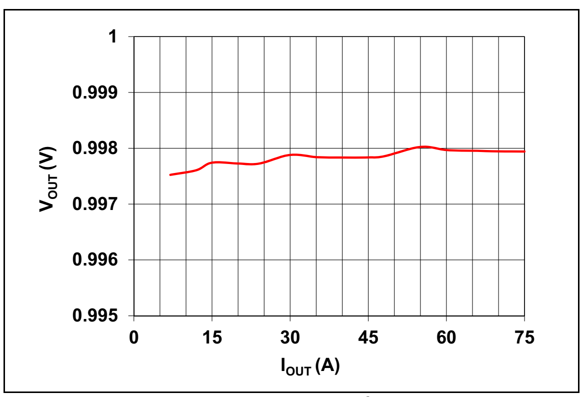


FIGURE 2-9: *Output Voltage vs. Input Voltage (V_{OUT} = 1V).*

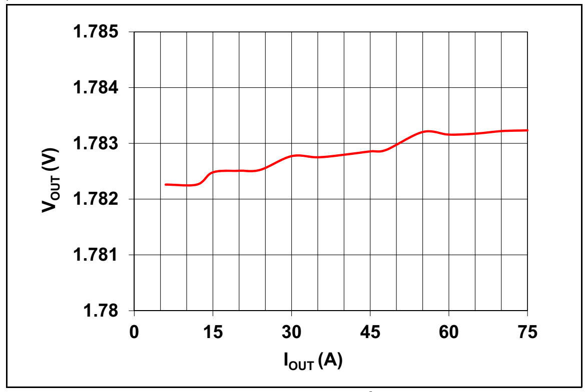


FIGURE 2-10: *Output Voltage vs. Input Voltage (V_{OUT} = 1.8V).*

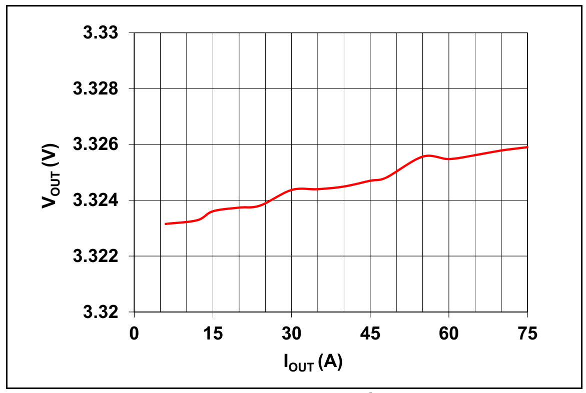


FIGURE 2-11: *Output Voltage vs. Input Voltage (V_{OUT} = 3.3V).*

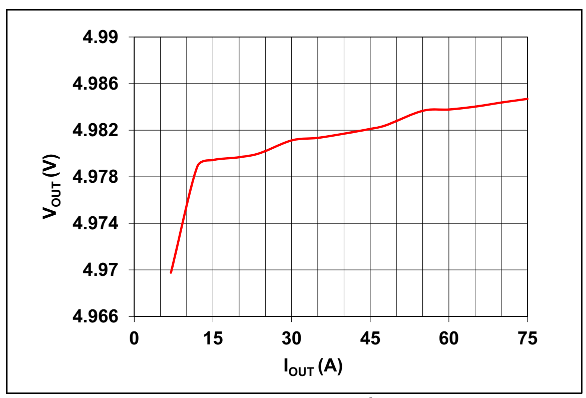


FIGURE 2-12: *Output Voltage vs. Input Voltage (V_{OUT} = 5V).*

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

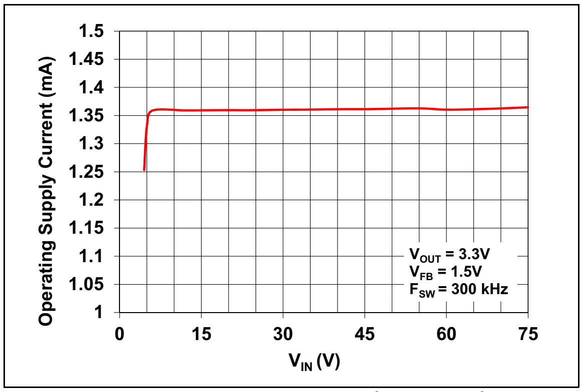


FIGURE 2-13: *V_{IN} Operating Supply Current vs. Input Voltage.*

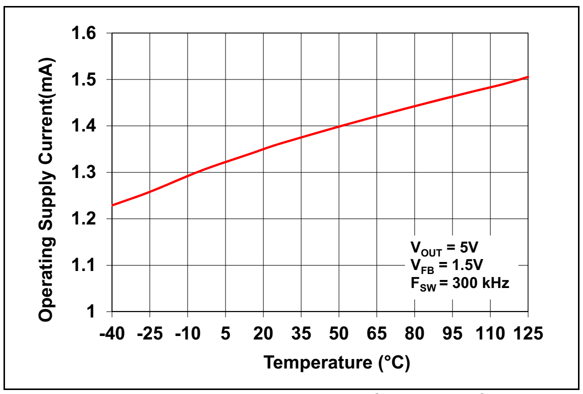


FIGURE 2-14: *V_{IN} Operating Supply Current vs. Temperature.*

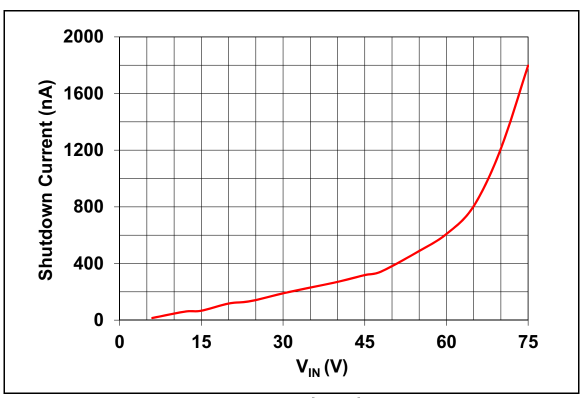


FIGURE 2-15: *V_{IN} Shutdown Current vs. Input Voltage.*

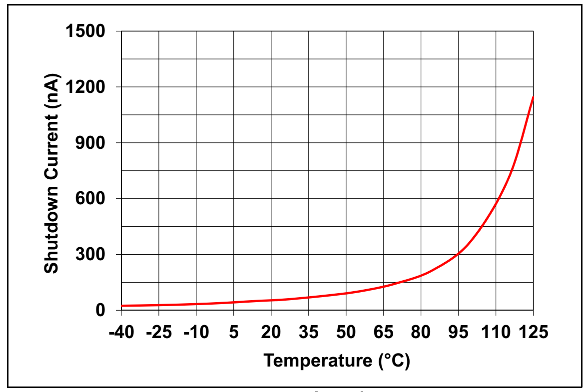


FIGURE 2-16: *V_{IN} Shutdown Current vs. Temperature.*

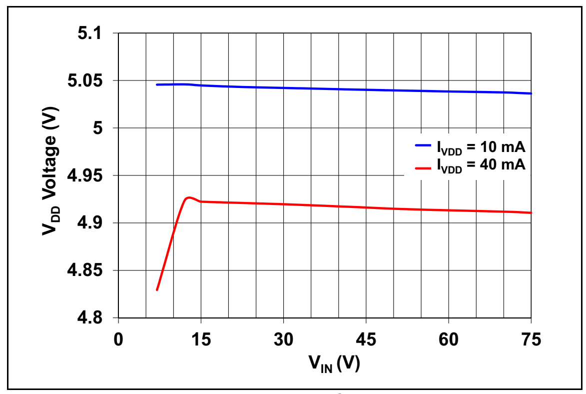


FIGURE 2-17: *V_{DD} Voltage vs. Input Voltage.*

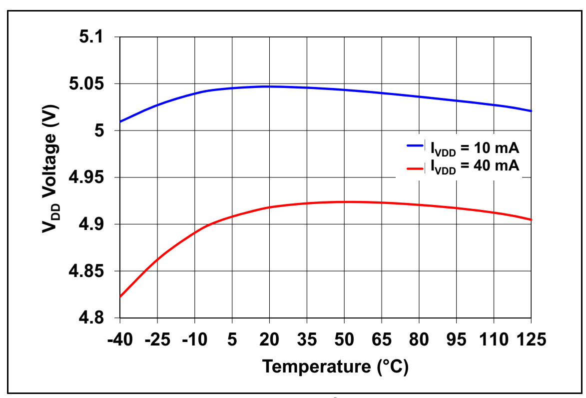


FIGURE 2-18: *V_{DD} Voltage vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

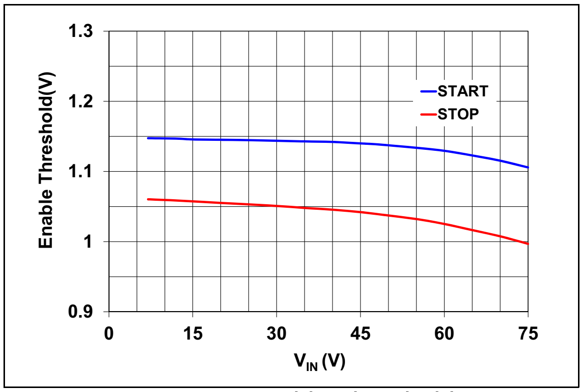


FIGURE 2-19: *Enable Threshold vs. Input Voltage.*

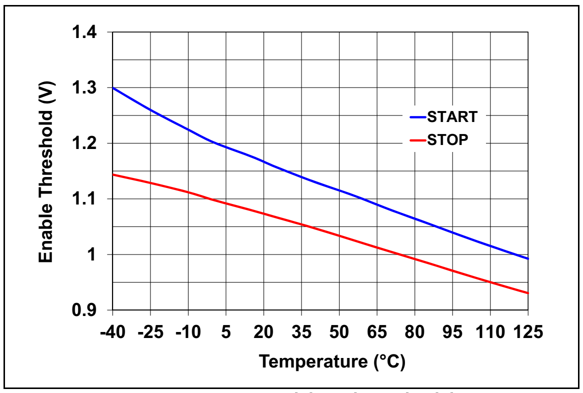


FIGURE 2-20: *Enable Threshold vs. Temperature.*

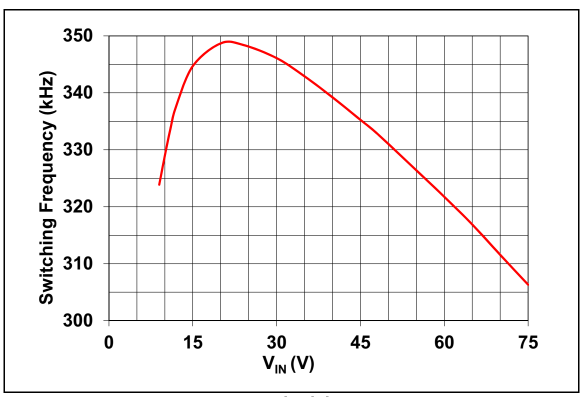


FIGURE 2-21: *Switching Frequency vs. Input Voltage.*

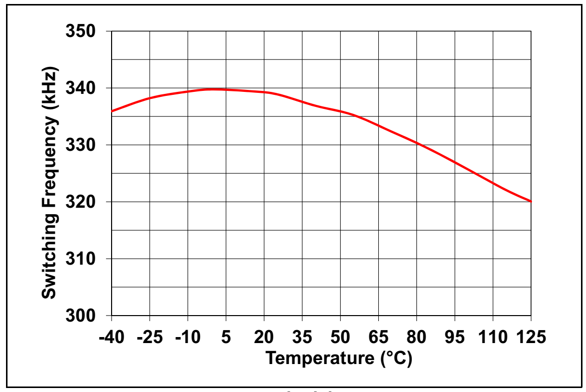


FIGURE 2-22: *Switching Frequency vs. Temperature.*

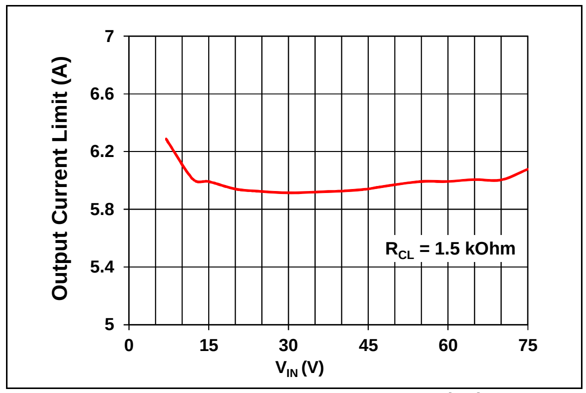


FIGURE 2-23: *Output Current Limit vs. Input Voltage.*

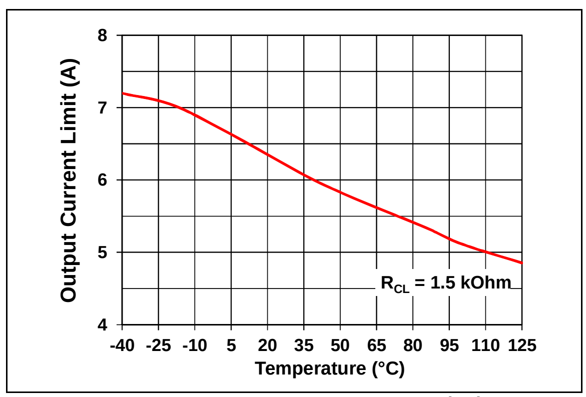


FIGURE 2-24: *Output Current Limit vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

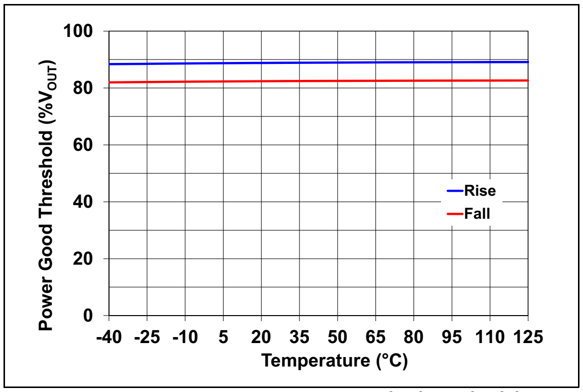


FIGURE 2-25: Power Good Threshold vs. Temperature.

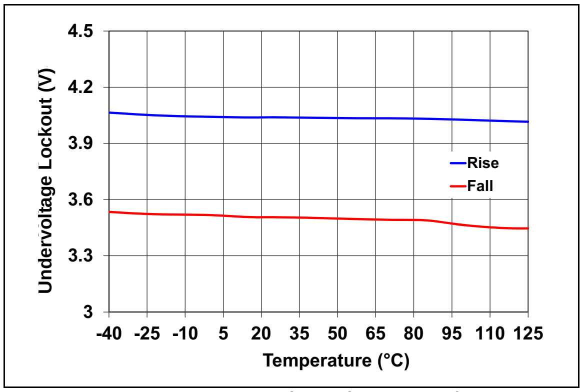


FIGURE 2-26: Undervoltage Lockout vs. Temperature.

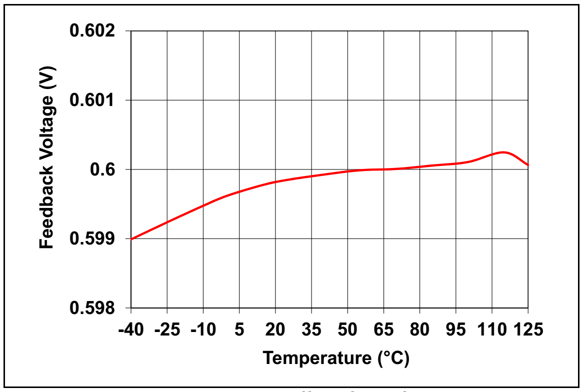


FIGURE 2-27: Feedback Voltage vs. Temperature.

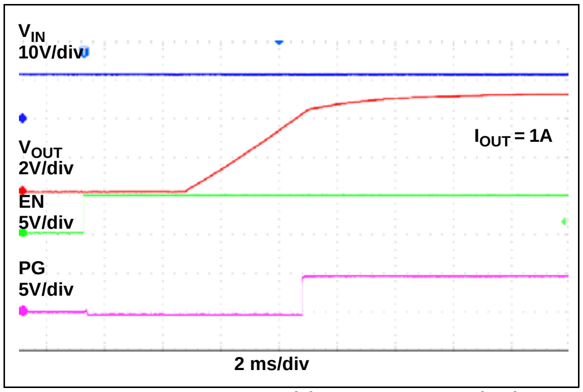


FIGURE 2-28: Enable Turn-On and Rise Time.

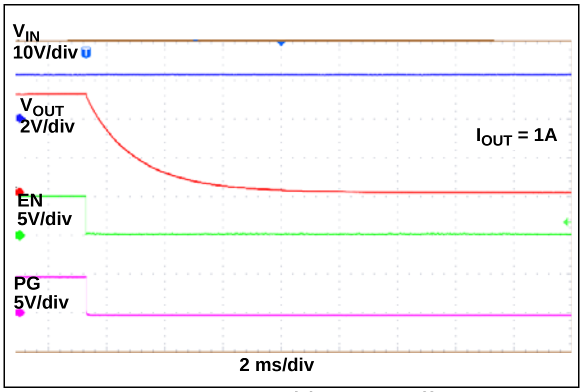


FIGURE 2-29: Enable Turn-Off.

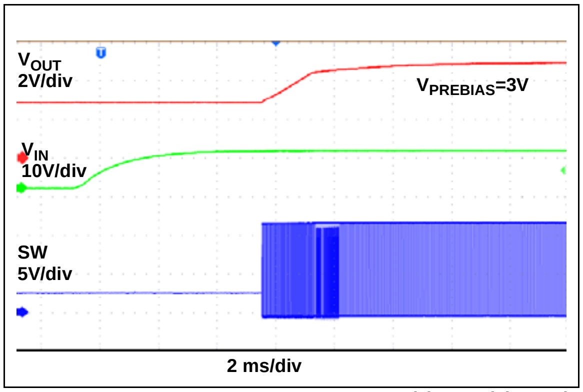


FIGURE 2-30: V_{IN} Start-up with Prebiased Output.

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

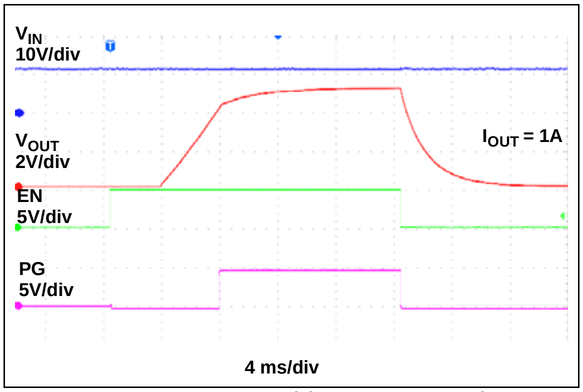


FIGURE 2-31: *Enable Turn-On and Turn-Off.*

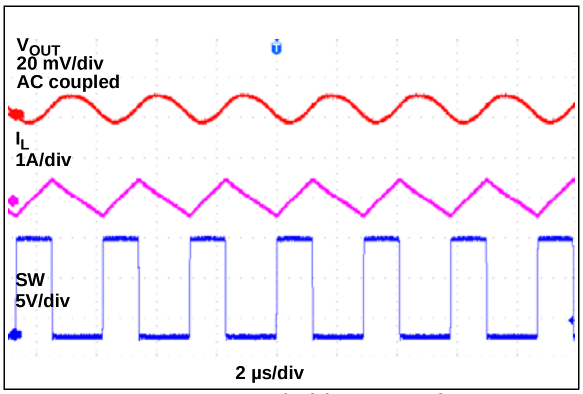


FIGURE 2-32: *Switching Waveform (I_{OUT} = 0A).*

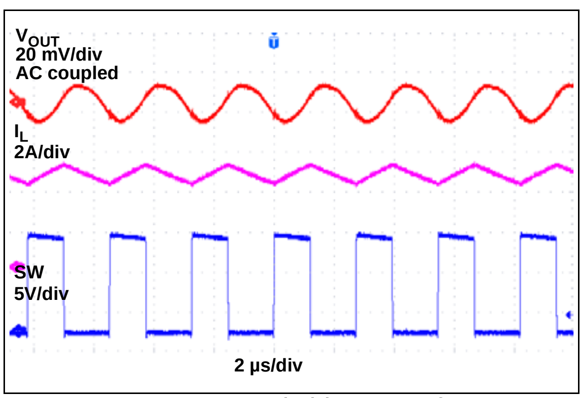


FIGURE 2-33: *Switching Waveform (I_{OUT} = 5A).*

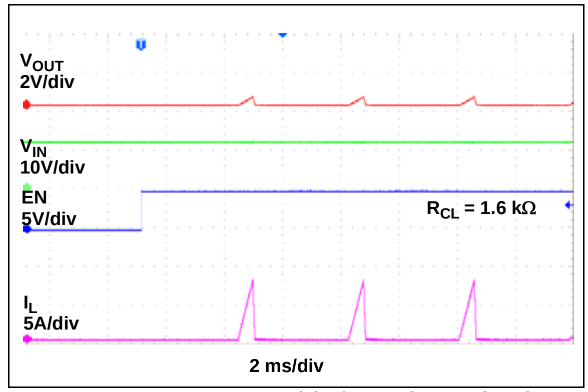


FIGURE 2-34: *Enable into Short Circuit.*

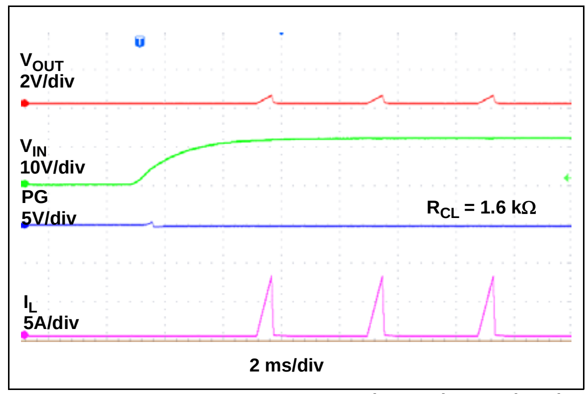


FIGURE 2-35: *Power-up into Short Circuit.*

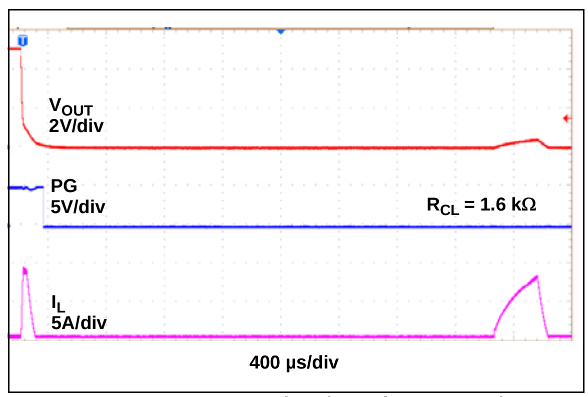


FIGURE 2-36: *Behavior when Entering Short Circuit.*

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

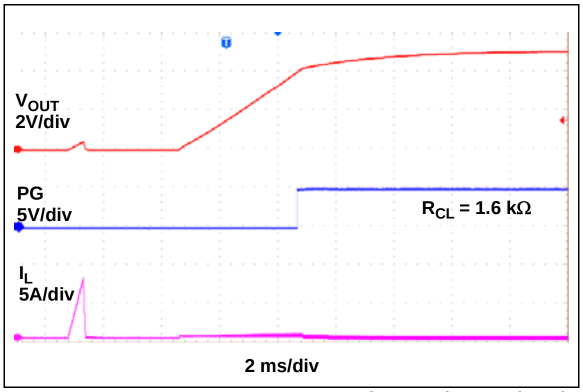


FIGURE 2-37: *Recovery from Short Circuit.*

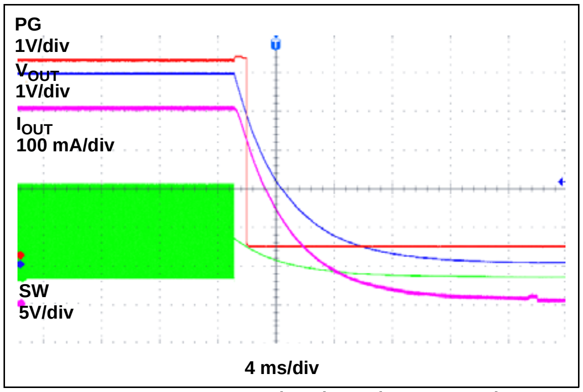


FIGURE 2-38: *Behavior when Entering Thermal Shutdown.*

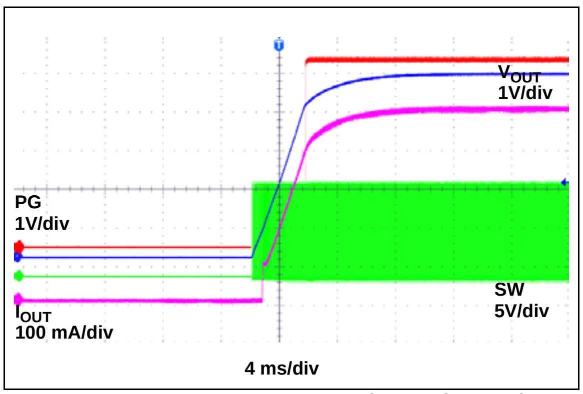


FIGURE 2-39: *Recovery from Thermal Shutdown.*

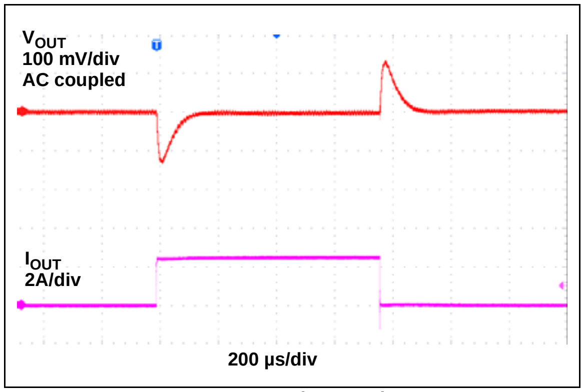


FIGURE 2-40: *Load Transient Response (0 to 2.5A).*

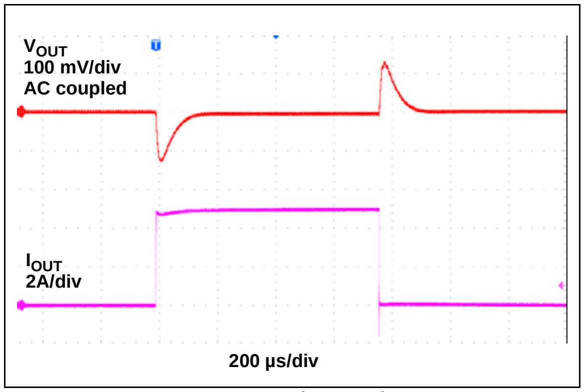


FIGURE 2-41: *Load Transient Response (0 to 5A).*

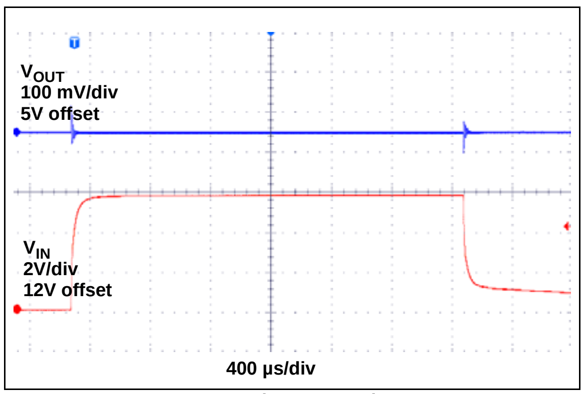


FIGURE 2-42: *Line Transient Response (12V to 18V).*

Note: Unless otherwise indicated, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 300 kHz, R_{CL} = 1.42 kΩ, L = 8.2 µH.

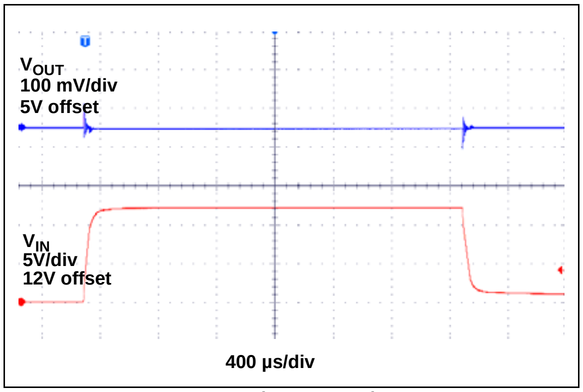


FIGURE 2-43: *Line Transient Response (12V to 24V).*

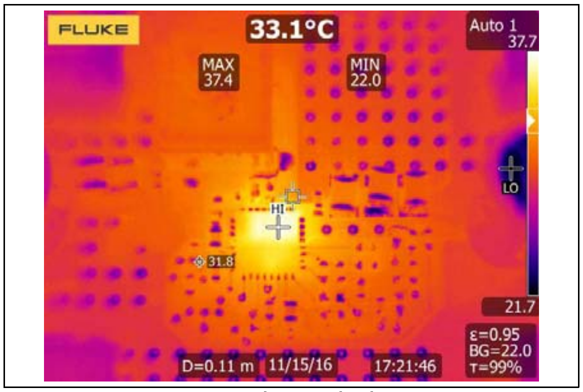


FIGURE 2-44: *Thermal Picture (I_{OUT} = 2.5A).*

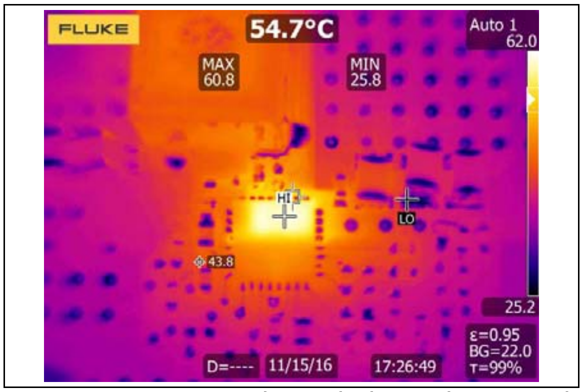


FIGURE 2-45: *Thermal Picture (I_{OUT} = 5A).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	I_{LIM}	Current Limit Adjust Input. Connect a resistor from I_{LIM} to the SW node to set the current limit. Refer to **Section 4.3 "Current Limit"** for more details.
2, 16, 17, 18, 19, 22, 29	PGND	Power Ground. PGND is the ground path for the MIC28514 buck converter power stage. The PGND pin connects to the sources of the low-side N-channel internal MOSFET, the negative terminals of the input capacitors and the negative terminals of the output capacitors. The loop for the Power Ground should be as small as possible and separate from the Analog Ground (AGND) loop.
3, 12, 13, 14, 15, 20	SW	Switch Node (Output). Internal connection for the high-side MOSFET source and low-side MOSFET drain. Connect one terminal of the Inductor to the SW node.
4	BST	Boost Pin (Output). Bootstrapped voltage to the high-side N-channel internal MOSFET driver. An internal diode is connected between the PV_{DD} pin and the BST pin. A boost capacitor of 0.1 µF is connected between the BST pin and the SW pin.
5, 6, 7, 8, 9, 10, 11	PV_{IN}	High-Side Internal N-Channel MOSFET Drain Connection (Input). The PV_{IN} operating voltage range is from 4.5V to 75V. Input capacitors between the PV_{IN} pins and the Power Ground (PGND) are required and the connection should be kept as short as possible.
21	PV_{DD}	Supply for the MOSFET Drivers. Connect to V_{DD} through a 2Ω series resistor. Connect a minimum 4.7 µF low-ESR ceramic capacitor from PV_{DD} to PGND.
23	EXTVDD	Auxiliary LDO Input. Connect to a supply higher than 4.7V (typical) to bypass the internal high-voltage LDO or leave unconnected/connected to ground. Connect a 2.2 µF low-ESR ceramic capacitor between EXTVDD and PGND when EXTVDD is connected to an external supply.
24	EN	Enable (Input). A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the OFF state, the V_{DD} supply current of the device is reduced. Do not pull the EN pin above the V_{DD} supply.
25	FREQ	Frequency Programming Input. Connect to V_{IN} to set the switching frequency to 800 kHz. Connect to the mid-point of a resistor divider from PV_{IN} to AGND to set the switching frequency. Refer to **Section 5.1 "Setting the Switching Frequency"**.
26	SS	Soft Start Adjustment Pin. Connect a capacitor from the SS pin to AGND to adjust the soft start time. See more details in **Section 5.0 "Application Information"**.
27	FB	Feedback (Input). Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.6V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
28	AGND	Analog Ground. Reference node for all the control logic circuits inside the MIC28514. Connect AGND to PGND at one point; see **Section 6.0 "PCB Layout Guidelines"** for details.
30	V_{DD}	V_{DD} Bias (Input). Power to the internal reference and control sections of the MIC28514. The V_{DD} operating voltage range is from 4.5V to 5.5V. A 2.2 µF ceramic capacitor from the V_{DD} pin to the PGND pin must be placed next to the IC.
31	SV_{IN}	Input Voltage to the internal regulator, which powers the internal reference and control section of the MIC28514. Connect to PV_{IN} through a 2Ω resistor. Connect a 1 µF capacitor from this pin to AGND.
32	PG	Open-Drain Power Good Output. PG is pulled to ground when the output voltage is below 90% of the target voltage. Pull-up to V_{DD} through a 10 kΩ resistor to set a logic high level when the output voltage is above 90% of the target voltage.

4.0 FUNCTIONAL DESCRIPTION

The MIC28514 is an adaptive on-time synchronous, step-down DC/DC regulator. It is designed to operate over a wide input voltage range, from 4.5V to 75V, and provides a regulated output voltage at up to 5A of output current. An adaptive on-time control scheme is employed in order to obtain a constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented with the use of an external sense resistor which sets the current limit. The device includes a programmable soft start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time.

4.1 Theory of Operation

The MIC28514 Functional Block Diagram appears on page 2. The output voltage is sensed by the MIC28514 Feedback pin, FB, via the voltage dividers, R1 and R2, and compared to a 0.6V reference voltage (V_{REF}), at the main comparator, through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier is below 0.6V, then the main comparator will trigger the control logic and generate an on-time period. The on-time period is predetermined by the fixed t_{ON} estimator circuitry value from Equation 4-1:

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output Voltage

V_{IN} = Power Stage Input Voltage

f_{SW} = Switching Frequency

At the end of the on-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The off-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.6V, the on-time period is triggered and the off-time period ends. If the off-time period, determined by the feedback voltage, is less than the minimum off-time, $t_{OFF(MIN)}$, which is about 240 ns, then the MIC28514 control logic will apply the $t_{OFF(MIN)}$ instead. The minimum $t_{OFF(MIN)}$ period is required to maintain enough energy in the Boost Capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 240 ns $t_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{240ns}{t_S}$$

Where:

t_S = $1/f_{SW}$

It is not recommended to use the MIC28514 with an off-time close to $t_{OFF(MIN)}$ during steady-state operation.

The actual on-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 75V to 1.0V.

Figure 4-1 shows the MIC28514 control loop timing during steady-state operation. During steady-state operation, the g_m amplifier senses the feedback voltage ripple. The feedback ripple is proportional to the output voltage ripple, and the inductor current ripple, to trigger the on-time period. The on-time is predetermined by the t_{ON} estimator. The termination of the off-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the off period ends and the next on-time period is triggered through the control logic circuitry.

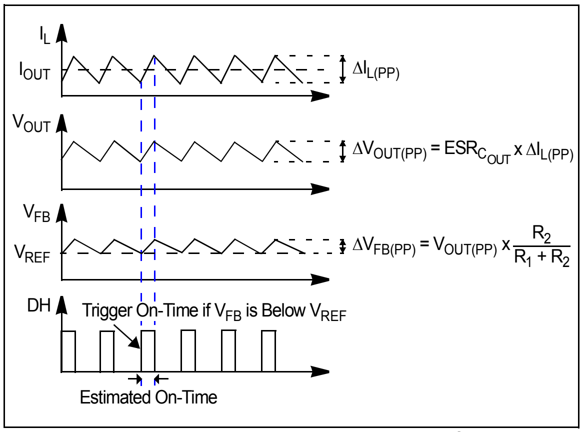


FIGURE 4-1: MIC28514 Control Loop Timing.

Figure 4-2 shows the operation of the MIC28514 during load transient. The output voltage drops due to the sudden load increase, which causes V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an on-time period. At the end of the on-time period, a minimum off-time is generated to charge C_{BST} because the feedback voltage is still below V_{REF}. Then, the next on-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC28514 converter.

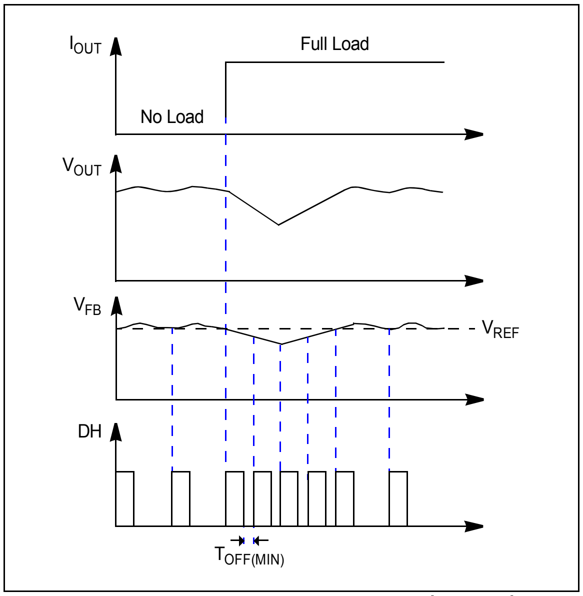


FIGURE 4-2: MIC28514 Load Transient Response.

Unlike true Current-mode control, the MIC28514 uses the output voltage ripple to trigger an on-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC28514 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier. The recommended feedback voltage ripple is 20 mV ~ 100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. For these applications, ripple injection is required to ensure proper operation. Refer to **Section 5.8 "Ripple Injection"** under **Section 5.0 "Application Information"** for details about the ripple injection technique.

4.2 Soft Start

Soft start reduces the power supply input surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC28514 features an adjustable soft start time. The soft start time can be adjusted by adjusting the value of the capacitor connected from the SS pin to AGND. The soft start time can be adjusted from 5 ms to 100 ms. The MIC28514 forces 1.4 µA current from the SS pin. This constant current flows through the capacitor connected from the SS pin to AGND to adjust the soft start time.

4.3 Current Limit

The MIC28514 uses the low-side MOSFET $R_{DS(ON)}$ to sense the inductor current. In each switching cycle of the MIC28514 converter, the inductor current is sensed by monitoring the voltage across the low-side MOSFET during the off period of the switching cycle, during which, the low-side MOSFET is on. An internal current source of 135 µA generates a voltage across the external Current Limit Setting Resistor, R_{CL}.

The I_{LIM} Pin Voltage (V_{ILIM}) is the difference of the voltage across the low-side MOSFET and the voltage across the resistor (V_{CL}). The sensed voltage, V_{ILIM},is compared with the Power Ground (PGND) after a blanking time of 150 ns.

If the absolute value of the voltage drop across the low-side MOSFET is greater than the absolute value of the voltage across the current setting resistor (V_{CL}), the MIC28514 triggers the current limit event. A consecutive eight current limit events trigger the Hiccup mode. Once the controller enters into Hiccup mode, it initiates a soft start sequence after a hiccup time-out of 4 ms (typical). Both the high-side and low-side MOSFETs are turned off during a hiccup time-out. The hiccup sequence, including the soft start, reduces the stress on the switching FETs, and protects the load and supply from severe short conditions.

Since the MOSFET $R_{DS(ON)}$ varies from 30% to 40% with temperature, it is recommended to consider the $R_{DS(ON)}$ variation, while calculating R_{CL} in the above equation, to avoid false current limiting due to increased MOSFET junction temperature rise.

To improve the current limit variation, the MIC28514 adjusts the internal Current Limit Source Current (I_{CL}) at a rate of 0.3 µA/°C when the MIC28514 junction temperature changes to compensate the $R_{DS(ON)}$ variation of the low-side MOSFET. Figure 2-23 indicates the temperature variation of the current limit with R_{CL}= 1.5 kΩ.

A small capacitor (C_{CL}) can be connected from the I_{LIM} pin to PGND to filter the switch node ringing during the off period, allowing a better current sensing. The time constant of R_{CL} and C_{CL} should be less than the minimum off-time.

4.4 Negative Current Limit

The MIC28514 implements a negative current limit by sensing the SW voltage when the low-side MOSFET is on. If the SW node voltage exceeds 48 mV, typical, or an equivalent of 2A, the device turns off the low-side MOSFET for 500 ns.

4.5 Internal MOSFET Gate Drive

The functional block diagram shows a bootstrap circuit, consisting of an internal diode from PV_{DD} to BST and an external capacitor connected from the SW pin to the BST pin (C_{BST}). This circuit supplies energy to the high-side drive circuit. Capacitor, C_{BST}, is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. Energy from C_{BST} is used to turn on the high-side MOSFET. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. The internal diode is reverse-biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10 mA, so a 0.1 µF to 1 µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle (i.e., ΔBST = 10 mA x 4 µs/0.1 µF = 400 mV). When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor in series with C_{BST} can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the PV_{DD} supply voltage. The nominal low-side gate drive voltage is PV_{DD} and the nominal high-side gate drive voltage is approximately PV_{DD} – V_{DIODE}, where V_{DIODE} is the voltage drop across the internal diode. An approximate 30 ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

4.6 Auxiliary Bootstrap LDO (EXTVDD)

The MIC28514 features an auxiliary bootstrap LDO which improves the system efficiency by supplying the MIC28514 internal circuit bias power and gate drivers from the converter output voltage. This LDO is enabled when the voltage on the EXTVDD pin is above 4.6V (typical), and at the same time, the main LDO which operates from V_{IN} is disabled to reduce power consumption.

5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC28514 is an adjustable frequency, synchronous buck regulator that features an adaptive on-time control architecture. The switching frequency can be adjusted between 270 kHz and 800 kHz by changing the resistor divider network, consisting of R_3 and R_4.

Equation 5-1 gives the estimated switching frequency.

EQUATION 5-1:

$$f_{SW(ADJ)} = f_O \times \frac{R_3}{R_3 + R_4}$$

Where:

f_O = Switching Frequency when R_4 is 100 kΩ and R_3 is open. f_O is typically 800 kHz.

5.2 Setting the Soft Start Time

The output soft start time can be set by connecting a capacitor from SS to AGND.

The value of the capacitor can be calculated using Equation 5-2.

EQUATION 5-2:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}$$

Where:

C_{SS} = Capacitor from SS pin to AGND

I_{SS} = Internal Soft Start Current(1.4 µA, typical)

t_{SS} = Output Soft Start Time

V_{REF} = 0.6V

5.3 Setting Output Voltage

The MIC28514 requires two resistors to set the output voltage, as shown in Figure 5-1.

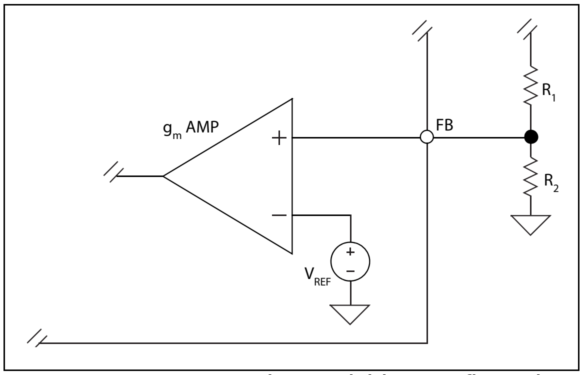


FIGURE 5-1: Voltage Divider Configuration.

The output voltage is determined by Equation 5-3:

EQUATION 5-3:

$$V_O = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where:

V_{FB} = 0.6V

A typical value of R_1 can be between 3 kΩ and 10 kΩ. If R_1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R_1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R_1 is selected, R_2 can be calculated using Equation 5-4.

EQUATION 5-4:

$$R_2 = \frac{V_{FB} \times R_1}{V_{OUT} - V_{FB}}$$

5.4 Setting the Current Limit

The Source Current Limit (I_{CL}) is trimmed at the factory to achieve a higher current limit accuracy with R_{CL} = 1.42 kΩ, as specified in Table 1-1 in **Section 1.0 "Electrical Characteristics"**. It is possible to adjust other current limits by changing the R_{CL} value using Equation 5-5.

EQUATION 5-5:

$$R_{CL} = \frac{\left(I_{LIM} + \frac{\Delta I_{L(PP)}}{2}\right) \times R_{DS(ON)}}{I_{CL}}$$

Where:

I_{LIM} = Load Current Limit

$R_{DS(ON)}$ = On-Resistance of the Low-Side MOSFET (25 mΩ, typical)

$\Delta I_{L(PP)}$ = Inductor Ripple Current

I_{CL} = Current Limit Source Current (135 µA, typical)

5.5 Inductor Selection

Values for inductance, peak and RMS currents are required to select the inductor. The input voltage, output voltage, switching frequency and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value, and therefore, a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 5-6.

EQUATION 5-6:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times 20\% \times I_{OUT(MAX)}}$$

Where:

f_{SW} = Switching Frequency

20% = Ratio of AC Ripple Current to DC Output Current

$V_{IN(MAX)}$ = Maximum Power Stage Input Voltage

For a selected inductor, the peak-to-peak inductor current ripple is:

EQUATION 5-7:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one-half of the peak-to-peak inductor current ripple.

EQUATION 5-8:

$$I_{L(PK)} = I_{OUT} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-9:

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires the proper selection of core material while minimizing the winding resistance. The high-frequency operation of the MIC28514 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower cost iron powder cores may be used, but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be significant. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-10.

EQUATION 5-10:

$$P_{INDUCTOR(CU)} = I_{L(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 5-11:

$$R_{WINDING(HT)} = R_{WINDING(20C)} \times (1 + 0.004 \times (T_H - T_{20C}))$$

Where:

T_H = Temperature of Wire Underload

T_{20C} = Ambient Temperature

$R_{WINDING(20C)}$ = Room Temperature Winding Resistance (usually specified by the manufacturer)

5.6 Output Capacitor Selection

The type of the output capacitor is usually determined by its Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON, and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of the ESR is calculated using Equation 5-12.

EQUATION 5-12:

$$ESR_{C_{OUT}} \le \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-Peak Output Voltage Ripple

$\Delta I_{L(PP)}$ = Peak-to-Peak Inductor Current Ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-13.

EQUATION 5-13:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + (\Delta I_{L(PP)} \times ESR_{C_{OUT}})^2}$$

Where:

C_{OUT} = Output Capacitance Value

f_{SW} = Switching Frequency

As described in **Section 4.1 "Theory of Operation"**, a subsection of **Section 4.0 "Functional Description"**, the MIC28514 requires at least 20 mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors' value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Refer to **Section 5.8 "Ripple Injection"** for details.

The voltage rating of the capacitor should be 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-14.

EQUATION 5-14:

$$I_{C_{OUT(RMS)}} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-15:

$$P_{DISS(COUT)} = I_{COUT(RMS)}{}^2 \times ESR_{COUT}$$

5.7 Input Capacitor Selection

The input capacitor for the power stage input, V_{IN}, should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents caused by turning on the input supply. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-16:

$$\Delta V_{IN} = I_{L(PK)} \times C_{ESR}$$

The input capacitor must be rated for the input current ripple. The RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-17:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-18:

$$P_{DISS(CIN)} = I_{CIN(RMS)}{}^2 \times C_{ESR}$$

5.8 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC28514 g_m amplifier and comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For low output voltages, such as 1V, the output voltage ripple is only 10 mV to 20 mV and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the g_m amplifier and comparator cannot sense it, then the MIC28514 loses control and the output voltage is not regulated. In order to have sufficient V_{FB} ripple, a ripple injection method should be applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors (Figure 5-2). The converter is stable without any ripple injection.

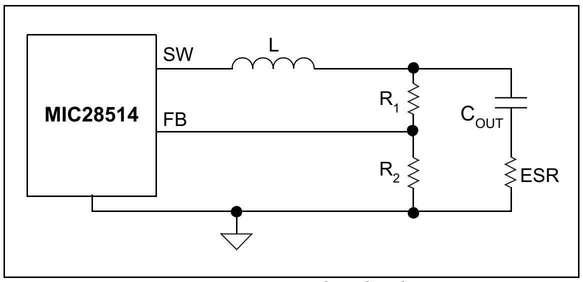


FIGURE 5-2: *Enough Ripple at FB.*

The feedback voltage ripple is:

EQUATION 5-19:

$$\Delta V_{FB(PP)} = \frac{R_2}{R_1 + R_2} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$ = Peak-to-Peak Value of the Inductor Current Ripple

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

   In this situation, the output voltage ripple is fed into the FB pin through a Feed-Forward Capacitor, C_{ff}, as shown in Figure 5-3. The typical C_{ff} value is between 1 nF and 22 nF.

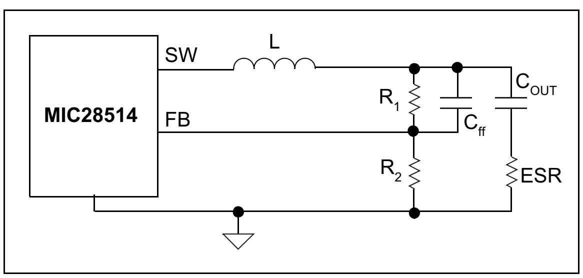


FIGURE 5-3: *Inadequate Ripple at FB.*

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple.

EQUATION 5-20:

$$\Delta V_{FB(PP)} \approx ESR_{COUT} \times \Delta I_{L(PP)}$$

3. Virtually no ripple at the FB pin voltage due to the very low-ESR of the output capacitors.

   In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the Switching Node, SW, via a resistor, R_{INJ}, and a capacitor, C_{INJ}, as shown in Figure 5-4.

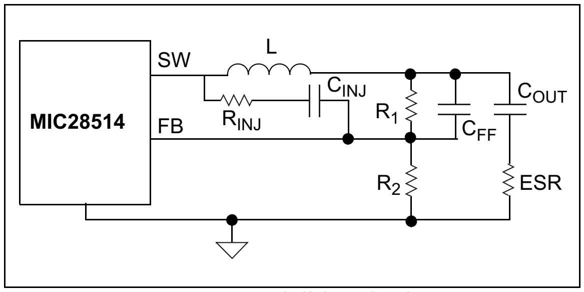


FIGURE 5-4: *Invisible Ripple at FB.*

The injected ripple is:

EQUATION 5-21:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:

V_{IN} = Power Stage Input Voltage

D = Duty Cycle

f_{SW} = Switching Frequency

τ = $(R_1//R_2//R_{INJ}) \times C_{ff}$

EQUATION 5-22:

$$K_{DIV} = \frac{R1//R2}{R_{INJ} + R1//R2}$$

In Equation 5-21 and Equation 5-22, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

EQUATION 5-23:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors, R1 and R2, are in the kΩ range, a C_{ff} of 1 nF to 22 nF can easily satisfy the large time constant requirements. Also, a 100 nF Injection Capacitor, C_{INJ}, is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is as follows.

1. Select C_{ff} to feed all output ripples into the Feedback pin and make sure the large time constant assumption is satisfied. A typical choice for C_{ff} is 1 nF to 22 nF if R_1 and R_2 are in the kΩ range.
2. Select R_{INJ} according to the expected feedback voltage ripple using Equation 5-24:

EQUATION 5-24:

$$K_{DIV} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

Then, the value of R_{INJ} is obtained as:

EQUATION 5-25:

$$R_{INJ} = (R1//R2) \times \left(\frac{1}{K_{DIV}} - 1\right)$$

3. Select C_{INJ} as 100 nF, which could be considered as short for a wide range of the frequencies.

5.9 Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermocouple that comes with a thermal meter. This thermocouple wire gauge is large, typically 22 gauge, and behaves like a heat sink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermocouple wire or an infrared thermometer. If a thermocouple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat sinking effect. In addition, the thermocouple tip must be covered in either thermal grease or thermal glue to make sure that the thermocouple junction is making good contact with the case of the IC.

Wherever possible, an infrared thermometer is recommended. An optional stand makes it easy to hold the beam on the IC for long periods of time.

6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The thickness of the copper planes is also important in terms of dissipating heat. The 2 oz. copper thickness is adequate from a thermal point of view and a thick copper plain helps in terms of noise immunity. Keep in mind, thinner planes can be easily penetrated by noise. The following guidelines should be followed to ensure proper operation of the MIC28514 converter.

6.1 IC

- The 2.2 µF ceramic capacitor, which is connected to the V_{DD} pin, must be located right at the IC. The V_{DD} pin is very noise-sensitive and placement of the capacitor is very critical. Use wide traces to connect to the V_{DD} pin.
- The Signal Ground pin (SGND) must be connected directly to the ground planes. The SGND and PGND connection should be done at a single point near the IC. Do not route the SGND pin to the PGND pad on the top layer.
- Use thick traces to route the input and output power lines.

6.2 Input Capacitor

- Place the input capacitor next to the power pins.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PV_{IN} pin and PGND connections short.
- Place several vias to the ground plane, close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U-type capacitors.
- If a tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In hot-plug applications, a tantalum or electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3 Inductor

- Keep the inductor connection to the Switch Node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the Switch Node (SW) away from the Feedback (FB) pin.

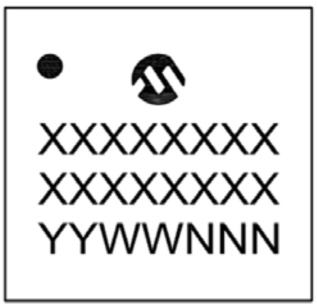
6.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

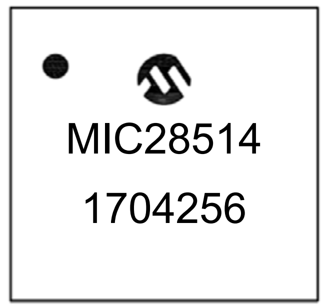
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

32-Pin VQFN (6 x 6 mm)



Example

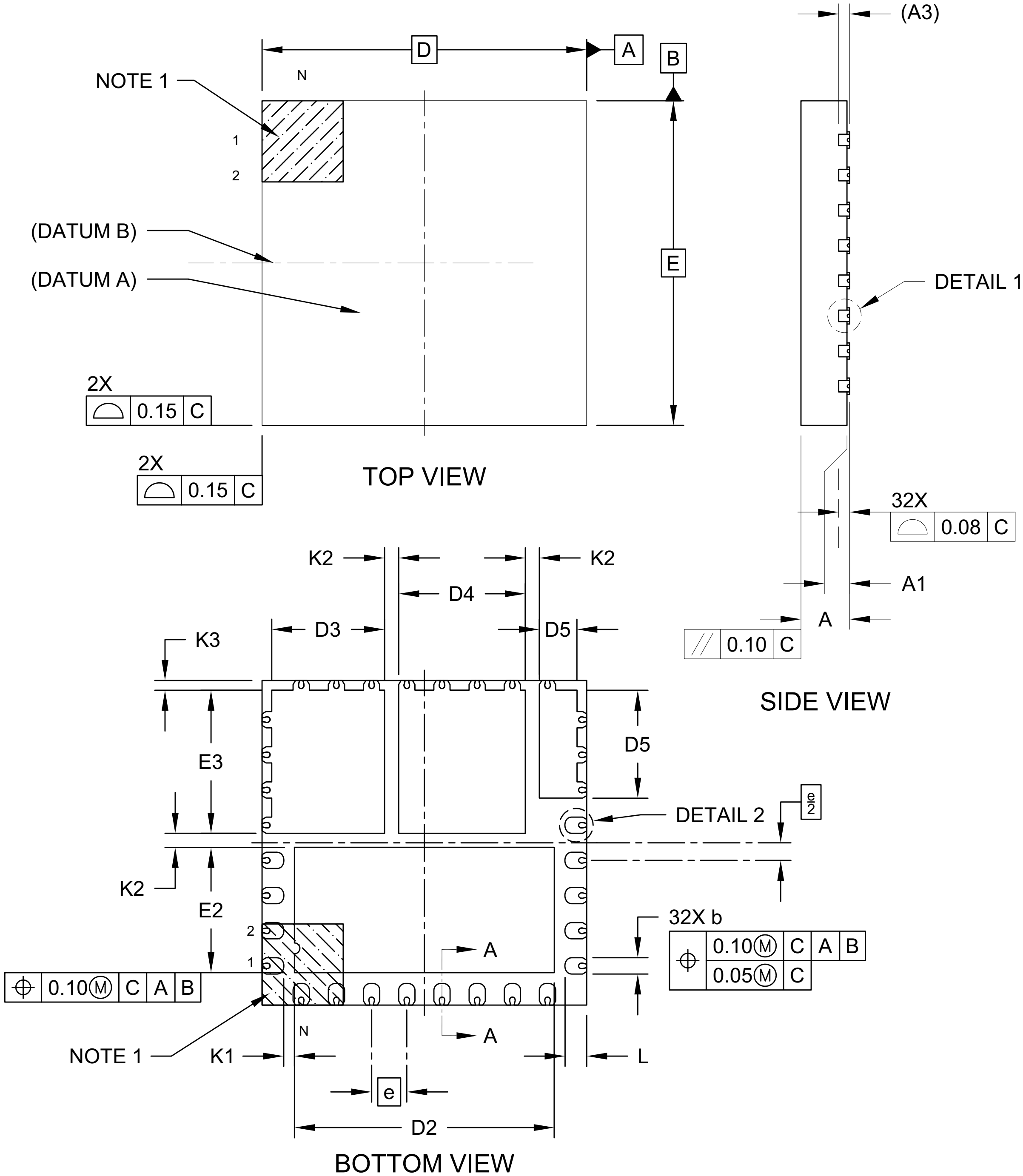


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32-Lead Very Thin Plastic Quad Flat, No Lead Package (PHA) - 6x6 mm Body [VQFN] Wettable Flanks, Multiple Exposed Pads

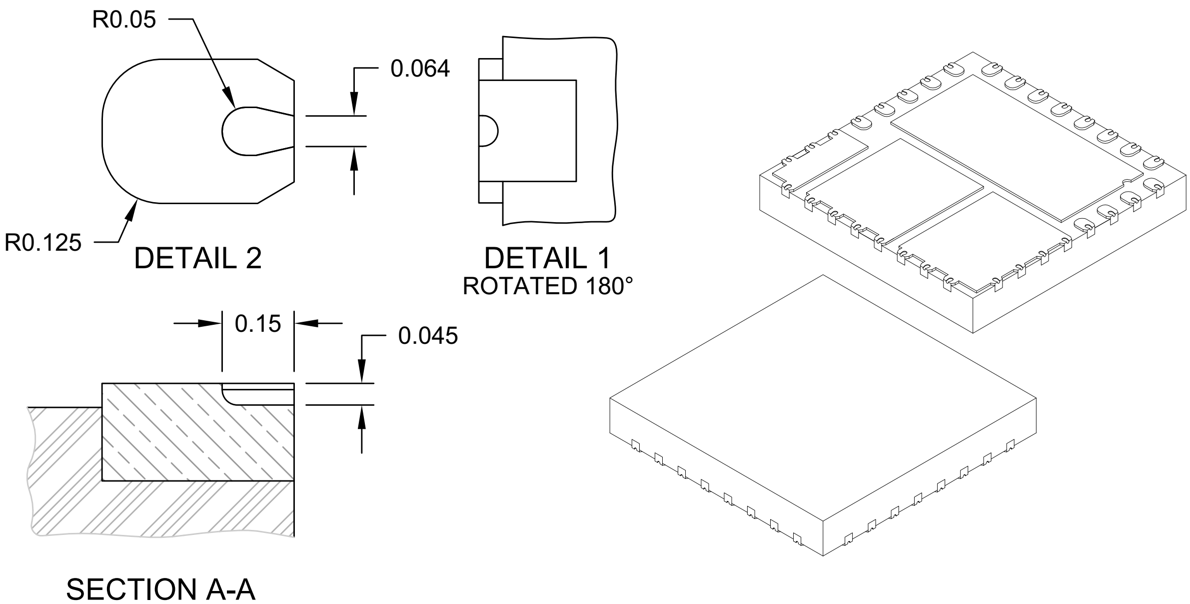
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1196A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (PHA) - 6x6 mm Body [VQFN] Wettable Flanks, Multiple Exposed Pads

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	4.70	4.80	4.90
Exposed Pad Width	E2	2.215	2.315	2.415
Exposed Pad Length	D3	1.985	2.085	2.185
Exposed Pad Width	E3	2.545	2.645	2.745
Exposed Pad Length	D4	2.240	2.340	2.440
Exposed Pad Length	D5	0.595	0.695	0.795
Exposed Pad Width	E5	1.895	1.995	2.095
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K1	0.20	-	-
Exposed Pad-to-Exposed Pad	K2	0.20	0.26	-
Pacakge Edgel-to-Exposed Pad	K3	0.18	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

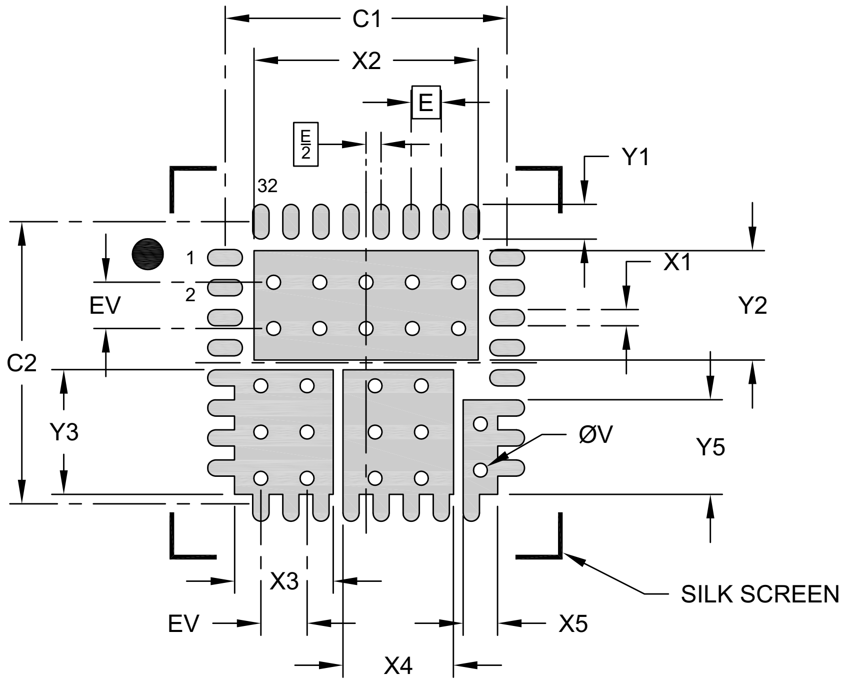
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1196A Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (PHA) - 6x6 mm Body [VQFN] Wettable Flanks, Multiple Exposed Pads

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Width (X32)	X1			0.35
Contact Pad Length (X32)	Y1			0.75
Contact Pad Spacing	C1		6.10	
Contact Pad Spacing	C2		6.10	
Inner Pad Length	X2			4.85
Inner Pad Width	Y2			2.36
Inner Pad Length	X3			2.13
Inner Pad Width	Y3			2.69
Inner Pad Length	X4			2.39
Inner Pad Length	X5			0.74
Inner Pad Width	Y5			2.04
Thermal Via Diameter (X26)	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3196A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2017)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	XXX
Device	Media Type	Temperature	Package

Device:	MIC28514T: 75V, 5A Hyper Speed Control® Synchronous DC/DC Buck Regulator with External Soft Start		
Media Type:	T	=	5000/Reel
Temperature:	E	=	Extended Temperature Range (-40°C to +125°C)
Package:	PHA	=	32-Lead, 6x6 mm VQFN

Examples:

a) MIC28514T-E/PHA: 75V, 5A Synchronous Buck Regulator, Hyper Speed Control® with Soft Start, -40°C to +125°C, Extended Temperature Range, 32-Lead QFN package

NOTES:

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