NimbeLink Hardware Design Checklist

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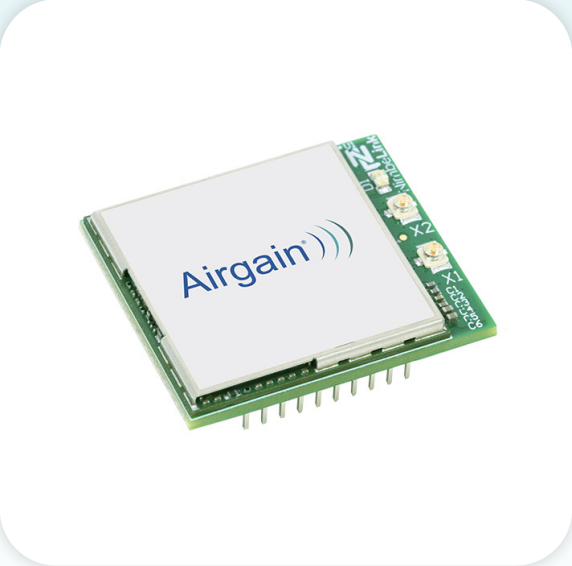

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1. Introduction

1.1 Scope

This document serves as a hardware design checklist for customers who are integrating Airgain's NimbeLink modems into their products. Included in this document is a checklist of important design considerations, as well as suggestions and tips for improving designs utilizing NimbeLink modems.

1.2 Orderable Devices

NimbeLink Family	Orderable Device
CAT-M1 LTE	NL-SW-LTE-QBG96 NL-SW-LTE-SVZM20 NL-SW-LTE-SVZM20-B NL-SW-LTE-TM1G-V NL-SW-LTE-TM1G-A
CAT-4 LTE	NL-SW-LTE-S7588-V NL-SW-LTE-S7588-V-B NL-SW-UAV-S7588 NL-SW-LTE-S7588-T NL-SW-LTE-S7588-T-C NL-SW-LTE-TC4NAG NL-SW-LTE-TC4APG NL-SW-LTE-TC4EU
CAT-3 LTE	NL-SW-LTE-TSVG NL-SW-LTE-TSVG-B NL-SW-LTE-TEUG NL-SW-LTE-TNAG NL-SW-LTE-TNAG-B
CAT-1 LTE	NL-SW-LTE-WM14 NL-SW-LTE-WM14-B NL-SW-LTE-WM14-C NL-SW-LTE-S7648 NL-SW-LTE-GELS3 NL-SW-LTE-GELS3-B NL-SW-LTE-GELS3-C NL-SW-LTE-GELS3-D NL-SW-LTE-S7618RD
Global 3G	NL-SW-HSPA

2. Design Checklist

2.1 Introduction

The following sections serve as a design checklist for NimbeLink modems. In order to properly create a design utilizing a cellular modem, it is crucial to account for each of the items listed in the checklist.

2.2 Pin Implementation Considerations

Each of the pins on the NimbeLink must be accounted for. Refer to the datasheet for the NimbeLink in question, and ensure that each pin is implemented according to the specifications listed in the datasheet.

Pin #	Pin Name	Requirements	Done?
1	VCC	The chosen power supply can supply up to 2 A of current at any time with minimal voltage drop during current spikes. • The power supply's output voltage must not drop outside of the modems operating voltage range at any time.	☐
		The chosen power supply has a rapid transient response. • It is recommended to use a switching power supply with a switching frequency > 1MHz. LDO's are not recommended.	☐
		A 0.1 µF capacitor should be placed nearest to the VCC pin, followed by a 100 µF capacitor. • Both capacitors are placed directly in the power path, and not off to the side. • Both capacitors must have low ESR.	☐
		PCB traces from the power regulator are wide enough to ensure that there is a low impedance power delivery circuit available to the modem. • It is recommended that the power supply traces be at least 80 mils wide on outer layers.	☐
		Noise sensitive signal lines (such as USB or RF signals) are insulated from the power supply input cables.	☐
		For any power traces that transition between PCB layers, multiple vias are used at each transition point. • It is recommended to use at least 4 vias for each trace that transitions across PCB layers.	☐
		Power and Ground pins have a continuous connection to their respective planes. Thermal reliefs are not recommended on these pins.	☐

2	**DOUT**	• If UART is used, the DOUT pin is implemented. • If UART is not used, DOUT is connected to a test pad.	☐
3	**DIN**	• If UART is used, the DIN pin is implemented. • If UART is not used, DIN is connected to a test pad.	☐
4, 10, 11, 15	**GND**	• If the PCB contains 4 or more layers, a dedicated ground plane is implemented. • Otherwise, if the PCB contains 2 or fewer layers, a ground plane has been properly implemented by creating a ground flood on all unused space.	☐
		• Unused space on non-ground plane layers are filled with ground and stitched together using stitching vias.	☐
5	**Reset**	• The Reset pin is implemented, and must be driven with an open collector output from the host system or with a discrete open collector transistor.	☐
6	**VUSB**	• If the USB interface is used the VUSB pin is connected to USB connector or on board USB controller. • If the USB interface is not used connect to test point.	☐
7, 8	**USB_D+ USB_D-**	If USB is being utilized, the USB D+ and USB D- are implemented.	☐
		The USB D± traces are routed as a 90 ohm impedance differential pair.	☐
		The USB D± traces are length matched.	☐
		The length of the USB D± traces is minimized as much as possible.	☐
		The USB differential pairs are routed such that there exists a continuous ground return path beneath the traces.	☐
		Any layer transition has multiple ground vias, for the current return path, next to the layer transition.	☐
		The USB trace is not routed over any splits in the directly adjacent ground plane	☐
		If the USB signals are being used off-board, ESD protection is implemented near the off-board connector.	☐
		There are no stubs in the signal path of the USB D± traces. If stubs are unavoidable length is <50mil.	☐
		The USB traces are not shared with any other device, populated or otherwise.	

9	**WAKE** (low to high) SVZM20 **nWAKE_IN** (pull down) WM14 DTR (Tie to GND)	Pin 9 is implemented and there exists a way to assert a logic state on this pin. • If Pin 9 is not actively controlled by the host system a 1 KOhm pull down resistor should be connected.	☐
12	**CTS**	The CTS pin is implemented, and there exists a way to read the logic state of this pin. • If the serial interface is not implemented, connect to test point.	☐
13	**STATUS** QBG96 **ON_STATUS** SVZM20 **VGPIO** S7588, S7648, S7618RD V180 GELS3 **ON/nSLEEP** TM1G, TSVG, TEUG, TNAG, HSPA, TC4NAG, TC4APG, TC4EU **nWAKE_OUT** WM14	Pin 13 is implemented, and there exists a way to read the logic state of this pin.	☐
14	**VREF**	A reference voltage has supplied to this pin and is in the appropriate voltage range for the UART signals.	☐
		A mechanism is in place that allows VREF to be disconnected from the NimbeLink. Used to achieve the lowest power states. • One way to achieve this is to use a GPIO to drive VREF, or to include aP-channel MOSFET in the VREF signal path to control the VREF signal from the host processor.	☐
16	**RTS**	The RTS pin is implemented, and there exists a way to assert a logic state on this pin. • If Pin 9 is not actively controlled by the host system, a 1 KOhm pull down resistor should be connected to the RTS pin.	☐

	I2C SDA QBG96	• Optional, leave floating if not used. • If implemented, the I2C SCL pin requires an external 1.8 V pullup.	☐
17	**DIOx** S7588, S7648, S7618RD,TM1G, TSVG, TEUG, TNAG, HSPA, GELS3 **GPIO3** TC4NAG, TC4APG, TC4EU **GPIO2** WM14	Optional, leave floating if not used.. • If implemented, ensure that the voltage on the pin is between 0 and 1.8V.	☐
	Reserved SVZM20	Pin 17 is not implemented, and is left floating.	☐
	I2C SCL QBG96	Optional, leave floating if not used. • If implemented, the I2C SCL pin requires an external 1.8 V pullup.	☐
18	**DIOx** S7588, S7648, S7618RD, GELS3, TM1G, TSVG, TEUG, TNAG, HSPA **GPIO2** TC4NAG, TC4APG, TC4EU **GPIO3** WM14	Optional, leave floating if not used. • If implemented, ensure that the voltage on the pin is between 0 and 1.8V.	☐
	Reserved SVZM20	Pin 18 is not implemented, and is left floating.	☐
19	**RING** QBG96, TM1G, SVZM20, TC4NAG, TC4APG, TC4NAG	• If the RING pin is implemented, there exists a way to read the logic state of this pin. • If the RING pin is not implemented, it is left floating or connect to a test point.	☐
	ADCI S7588, S7648, S7618RD,TSVG, TEUG, TNAG, HSPA, WM14, GELS3	Optional, leave floating if not used. • If implemented, ensure that the voltage on the pin is between 0 and 1.8V.	☐
20	**ON_OFF** or **PWR_ON**	Pin 20 is implemented and must be driven with an open collector output from the host system or with a discrete open collector transistor.	

2.3 Antenna Considerations

Design Considerations	Done?
An appropriate primary antenna has been selected for the NimbeLink. • Refer to the relevant NimbeLink datasheet for antenna design requirements, and recommended antennas.	☐
If required, a suitable diversity antenna has been chosen for the NimbeLink. • Refer to the relevant NimbeLink Datasheet for antenna design requirements, and recommended antennas.	☐
The antenna(s) are sufficiently isolated from noise generated by other design components.	☐
The antenna(s) are mounted in accordance with the manufacturer's guidelines.	☐

2.4 Enclosure Considerations

Design Considerations	Done?
The enclosure design insulates the NimbeLink from outdoor environments. • A sealed enclosure is recommended.	☐
The enclosure design ensures that the NimbeLink is protected from moisture. • Condensing moisture will permanently damage the modem. Check modem datasheet for acceptable range.	☐
The enclosure does not adversely affect the signal strength of the antenna(s). • Metal enclosures and metal objects will block and/or detune antenna systems. Consult an RF engineer for guidance on antenna selection and placement.	☐

2.4 Power Supply Considerations

Design Considerations	Done?
The power supply is designed to prevent brownout conditions from occurring. • Brownouts may damage the modem.	☐
The power supply layout is in accordance with the manufacturer's guidelines.	☐
Power supply switching current loops are minimized.	☐
The power supply is controlled in a manner such that the power will not be cut from the modem until modem has properly shut down.	☐
A mechanism is implemented that ensures the modem can always gracefully disconnect from the network in the event of a power failure.	☐

2.4 General Design Considerations

Design Considerations	Done?
Firmware update and debugging considerations: If USB is not used in the design, include a USB connector connected to NimbeLink USB interface so firmware can be updated on the modem while installed in the product. • Even if USB is unused in the final implementation, it is highly recommended that a connector be included in the final design for firmware updates and debugging purposes.	☐